

# Contents

<b>Foreword</b>	<b>xvii</b>
<b>Preface</b>	<b>xix</b>
<b>Acknowledgements</b>	<b>xxvii</b>
<b>1 VLSI Physical Design Automation</b>	<b>1</b>
1.1 VLSI Design Cycle . . . . .	3
1.2 New Trends in VLSI Design Cycle . . . . .	7
1.3 Physical Design Cycle . . . . .	9
1.4 New Trends in Physical Design Cycle . . . . .	13
1.5 Design Styles . . . . .	15
1.5.1 Full-Custom . . . . .	17
1.5.2 Standard Cell . . . . .	18
1.5.3 Gate Arrays . . . . .	20
1.5.4 Field Programmable Gate Arrays . . . . .	22
1.5.5 Sea of Gates . . . . .	25
1.5.6 Comparison of Different Design Styles . . . . .	25
1.6 System Packaging Styles . . . . .	26
1.6.1 Die Packaging and Attachment Styles . . . . .	26
1.6.1.1 Die Package Styles . . . . .	26
1.6.1.2 Package and Die Attachment Styles . . . . .	27
1.6.2 Printed Circuit Boards . . . . .	27
1.6.3 Multichip Modules . . . . .	29
1.6.4 Wafer Scale Integration . . . . .	31
1.6.5 Comparison of Different Packaging Styles . . . . .	31
1.7 Historical Perspectives . . . . .	32
1.8 Existing Design Tools . . . . .	33
1.9 Summary . . . . .	35
<b>2 Design and Fabrication of VLSI Devices</b>	<b>39</b>
2.1 Fabrication Materials . . . . .	40
2.2 Transistor Fundamentals . . . . .	43
2.2.1 Basic Semiconductor Junction . . . . .	43
2.2.2 TTL Transistors . . . . .	45

- 2.2.3 MOS Transistors . . . . . 46
- 2.3 Fabrication of VLSI Circuits . . . . . 48
  - 2.3.1 nMOS Fabrication Process . . . . . 51
  - 2.3.2 CMOS Fabrication Process . . . . . 53
  - 2.3.3 Details of Fabrication Processes . . . . . 53
- 2.4 Design Rules . . . . . 58
- 2.5 Layout of Basic Devices . . . . . 62
  - 2.5.1 Inverters . . . . . 62
  - 2.5.2 NAND and NOR Gates . . . . . 64
  - 2.5.3 Memory Cells . . . . . 66
    - 2.5.3.1 Static Random Access Memory (SRAM) . . . 67
    - 2.5.3.2 Dynamic Random Access Memory (DRAM) . 69
- 2.6 Summary . . . . . 71
- 2.7 Exercises . . . . . 71
- 3 Fabrication Process and its Impact on Physical Design 75**
  - 3.1 Scaling Methods . . . . . 76
  - 3.2 Status of Fabrication Process . . . . . 77
    - 3.2.1 Comparison of Fabrication Processes . . . . . 77
  - 3.3 Issues related to the Fabrication Process . . . . . 79
    - 3.3.1 Parasitic Effects . . . . . 79
    - 3.3.2 Interconnect Delay . . . . . 80
    - 3.3.3 Noise and Crosstalk . . . . . 81
    - 3.3.4 Interconnect Size and Complexity . . . . . 82
    - 3.3.5 Other Issues in Interconnect . . . . . 82
    - 3.3.6 Power Dissipation . . . . . 82
    - 3.3.7 Yield and Fabrication Costs . . . . . 83
  - 3.4 Future of Fabrication Process . . . . . 85
    - 3.4.1 SIA Roadmap . . . . . 85
    - 3.4.2 Advances in Lithography . . . . . 86
    - 3.4.3 Innovations in Interconnect . . . . . 87
      - 3.4.3.1 More Layers of Metal . . . . . 87
      - 3.4.3.2 Local Interconnect . . . . . 87
      - 3.4.3.3 Copper Interconnect . . . . . 87
      - 3.4.3.4 Unlanded Vias . . . . . 88
    - 3.4.4 Innovations/Issues in Devices . . . . . 88
    - 3.4.5 Aggressive Projections for the Process . . . . . 89
    - 3.4.6 Other Process Innovations . . . . . 90
      - 3.4.6.1 Silicon On Insulator . . . . . 90
      - 3.4.6.2 Silicon Germanium . . . . . 90
  - 3.5 Solutions for Interconnect Issues . . . . . 91
  - 3.6 Tools for Process Development . . . . . 93
  - 3.7 Summary . . . . . 94
  - 3.8 Exercises . . . . . 94

<b>4</b>	<b>Data Structures and Basic Algorithms</b>	<b>97</b>
4.1	Basic Terminology . . . . .	99
4.2	Complexity Issues and NP-hardness . . . . .	100
4.2.1	Algorithms for NP-hard Problems . . . . .	101
4.2.1.1	Exponential Algorithms . . . . .	102
4.2.1.2	Special Case Algorithms . . . . .	102
4.2.1.3	Approximation Algorithms . . . . .	102
4.2.1.4	Heuristic Algorithms . . . . .	103
4.3	Basic Algorithms . . . . .	104
4.3.1	Graph Algorithms . . . . .	104
4.3.1.1	Graph Search Algorithms . . . . .	104
4.3.1.2	Spanning Tree Algorithms . . . . .	106
4.3.1.3	Shortest Path Algorithms . . . . .	108
4.3.1.4	Matching Algorithms . . . . .	110
4.3.1.5	Min-Cut and Max-Cut Algorithms . . . . .	110
4.3.1.6	Steiner Tree Algorithms . . . . .	111
4.3.2	Computational Geometry Algorithms . . . . .	115
4.3.2.1	Line Sweep Method . . . . .	115
4.3.2.2	Extended Line Sweep Method . . . . .	115
4.4	Basic Data Structures . . . . .	117
4.4.1	Atomic Operations for Layout Editors . . . . .	117
4.4.2	Linked List of Blocks . . . . .	119
4.4.3	Bin-Based Method . . . . .	120
4.4.4	Neighbor Pointers . . . . .	122
4.4.5	Corner Stitching . . . . .	123
4.4.6	Multi-layer Operations . . . . .	130
4.4.7	Limitations of Existing Data Structures . . . . .	131
4.4.8	Layout Specification Languages . . . . .	131
4.5	Graph Algorithms for Physical design . . . . .	135
4.5.1	Classes of Graphs in Physical Design . . . . .	135
4.5.1.1	Graphs Related to a Set of Lines . . . . .	136
4.5.1.2	Graphs Related to Set of Rectangles . . . . .	138
4.5.2	Relationship Between Graph Classes . . . . .	138
4.5.3	Graph Problems in Physical Design . . . . .	140
4.5.4	Algorithms for Interval Graphs . . . . .	142
4.5.4.1	Maximum Independent Set . . . . .	142
4.5.4.2	Maximum Clique and Minimum Coloring . . . . .	143
4.5.5	Algorithms for Permutation Graphs . . . . .	144
4.5.5.1	Maximum Independent Set . . . . .	144
4.5.5.2	Maximum $k$ -Independent Set . . . . .	146
4.5.6	Algorithms for Circle Graphs . . . . .	148
4.5.6.1	Maximum Independent Set . . . . .	148
4.5.6.2	Maximum $k$ -Independent Set . . . . .	149
4.5.6.3	Maximum Clique . . . . .	151
4.6	Summary . . . . .	151
4.7	Exercises . . . . .	152

<b>5</b>	<b>Partitioning</b>	<b>157</b>
5.1	Problem Formulation . . . . .	163
5.1.1	Design Style Specific Partitioning Problems . . . . .	166
5.2	Classification of Partitioning Algorithms . . . . .	168
5.3	Group Migration Algorithms . . . . .	169
5.3.1	Kernighan-Lin Algorithm . . . . .	170
5.3.2	Extensions of Kernighan-Lin Algorithm . . . . .	171
5.3.2.1	Fiduccia-Mattheyses Algorithm . . . . .	173
5.3.2.2	Goldberg and Burstein Algorithm . . . . .	174
5.3.2.3	Component Replication . . . . .	174
5.3.2.4	Ratio Cut . . . . .	176
5.4	Simulated Annealing and Evolution . . . . .	177
5.4.1	Simulated Annealing . . . . .	177
5.4.2	Simulated Evolution . . . . .	179
5.5	Other Partitioning Algorithms . . . . .	183
5.5.1	Metric Allocation Method . . . . .	183
5.6	Performance Driven Partitioning . . . . .	185
5.7	Summary . . . . .	187
5.8	Exercises . . . . .	187
<b>6</b>	<b>Floorplanning and Pin Assignment</b>	<b>191</b>
6.1	Floorplanning . . . . .	193
6.1.1	Problem Formulation . . . . .	193
6.1.1.1	Design Style Specific Floorplanning Problems . . . . .	194
6.1.2	Classification of Floorplanning Algorithms . . . . .	194
6.1.3	Constraint Based Floorplanning . . . . .	196
6.1.4	Integer Programming Based Floorplanning . . . . .	198
6.1.5	Rectangular Dualization . . . . .	200
6.1.6	Hierarchical Tree Based Methods . . . . .	201
6.1.7	Floorplanning Algorithms for Mixed Block and Cell Designs . . . . .	203
6.1.8	Simulated Evolution Algorithms . . . . .	203
6.1.9	Timing Driven Floorplanning . . . . .	204
6.1.10	Theoretical advancements in Floorplanning . . . . .	205
6.1.11	Recent Trends . . . . .	206
6.2	Chip planning . . . . .	207
6.2.1	Problem Formulation . . . . .	207
6.3	Pin Assignment . . . . .	207
6.3.1	Problem Formulation . . . . .	208
6.3.1.1	Design Style Specific Pin Assignment Problems . . . . .	208
6.3.2	Classification of Pin Assignment Algorithms . . . . .	209
6.3.3	General Pin Assignment . . . . .	210
6.3.4	Channel Pin Assignment . . . . .	211
6.4	Integrated Approach . . . . .	214
6.5	Summary . . . . .	217
6.6	Exercises . . . . .	217

<b>7</b>	<b>Placement</b>	<b>219</b>
7.1	Problem Formulation . . . . .	220
7.1.1	Design Style Specific Placement Problems . . . . .	223
7.2	Classification of Placement Algorithms . . . . .	225
7.3	Simulation Based Placement Algorithms . . . . .	225
7.3.1	Simulated Annealing . . . . .	226
7.3.2	Simulated Evolution . . . . .	229
7.3.3	Force Directed Placement . . . . .	232
7.3.4	Sequence-Pair Technique . . . . .	233
	. . . . .	233
7.3.5	Comparison of Simulation Based Algorithms . . . . .	236
7.4	Partitioning Based Placement Algorithms . . . . .	236
7.4.1	Breuer’s Algorithm . . . . .	236
7.4.2	Terminal Propagation Algorithm . . . . .	239
7.5	Other Placement Algorithms . . . . .	240
7.5.1	Cluster Growth . . . . .	240
7.5.2	Quadratic Assignment . . . . .	241
7.5.3	Resistive Network Optimization . . . . .	241
7.5.4	Branch-and-Bound Technique . . . . .	242
7.6	Performance Driven Placement . . . . .	242
7.7	Recent Trends . . . . .	243
7.8	Summary . . . . .	244
7.9	Exercises . . . . .	244
<b>8</b>	<b>Global Routing</b>	<b>247</b>
8.1	Problem Formulation . . . . .	253
8.1.1	Design Style Specific Global Routing Problems . . . . .	257
8.2	Classification of Global Routing Algorithms . . . . .	260
8.3	Maze Routing Algorithms . . . . .	261
8.3.1	Lee’s Algorithm . . . . .	261
8.3.2	Soukup’s Algorithm . . . . .	263
8.3.3	Hadlock’s Algorithm . . . . .	264
8.3.4	Comparison of Maze Routing Algorithms . . . . .	267
8.4	Line-Probe Algorithms . . . . .	269
8.5	Shortest Path Based Algorithms . . . . .	272
8.6	Steiner Tree based Algorithms . . . . .	273
8.6.1	Separability Based Algorithm . . . . .	274
8.6.2	Non-Rectilinear Steiner Tree Based Algorithm . . . . .	277
8.6.3	Steiner Min-Max Tree based Algorithm . . . . .	279
8.6.4	Weighted Steiner Tree based Algorithm . . . . .	281
8.7	Integer Programming Based Approach . . . . .	282
8.7.1	Hierarchical Approach . . . . .	282
8.8	Performance Driven Routing . . . . .	286
8.9	Summary . . . . .	287
8.10	Exercises . . . . .	288

<b>9 Detailed Routing</b>	<b>291</b>
9.1 Problem Formulation . . . . .	293
9.1.1 Routing Considerations . . . . .	293
9.1.2 Routing Models . . . . .	295
9.1.3 Channel Routing Problems . . . . .	297
9.1.4 Switchbox Routing Problems . . . . .	302
9.1.5 Design Style Specific Detailed Routing Problems . . . . .	302
9.2 Classification of Routing Algorithms . . . . .	303
9.3 Single-Layer Routing Algorithms . . . . .	304
9.3.1 General River Routing Problem . . . . .	306
9.3.1.1 General River Routing Algorithm . . . . .	306
9.3.2 Single Row Routing Problem . . . . .	311
9.3.2.1 Origin of Single Row Routing . . . . .	312
9.3.2.2 A Graph Theoretic Approach . . . . .	316
9.3.2.3 Algorithm for Street Congestion Minimization . . . . .	316
9.3.2.4 Algorithm for Minimizing Doglegs . . . . .	318
9.4 Two-Layer Channel Routing Algorithms . . . . .	320
9.4.1 Classification of Two-Layer Algorithms . . . . .	320
9.4.2 LEA based Algorithms . . . . .	321
9.4.2.1 Basic Left-Edge Algorithm . . . . .	321
9.4.2.2 Dogleg Router . . . . .	323
9.4.2.3 Symbolic Channel Router: YACR2 . . . . .	325
9.4.3 Constraint Graph based Routing Algorithms . . . . .	329
9.4.3.1 Net Merge Channel Router . . . . .	330
9.4.3.2 Glitter: A Gridless Channel Router . . . . .	334
9.4.4 Greedy Channel Router . . . . .	338
9.4.5 Hierarchical Channel Router . . . . .	340
9.4.6 Comparison of Two-Layer Channel Routers . . . . .	345
9.5 Three-Layer Channel Routing Algorithms . . . . .	345
9.5.1 Classification of Three-Layer Algorithms . . . . .	346
9.5.2 Extended Net Merge Channel Router . . . . .	346
9.5.3 HVH Routing from HV Solution . . . . .	348
9.5.4 Hybrid HVH-VHV Router . . . . .	349
9.6 Multi-Layer Channel Routing Algorithms . . . . .	352
9.7 Switchbox Routing Algorithms . . . . .	353
9.7.1 Classification of switchbox routing algorithms . . . . .	354
9.7.2 Greedy Router . . . . .	355
9.7.3 Rip-up and Re-route Based Router . . . . .	358
9.7.4 Computational Geometry Based Router . . . . .	358
9.7.5 Comparison of Switchbox Routers . . . . .	362
9.8 Summary . . . . .	362
9.9 Exercises . . . . .	363

**10 Over-the-Cell Routing and Via Minimization 369**

- 10.1 Over-the-cell Routing . . . . . 370
  - 10.1.1 Cell Models . . . . . 371
  - 10.1.2 Two-Layer Over-the-Cell Routers . . . . . 373
    - 10.1.2.1 Basic OTC Routing Algorithm . . . . . 373
    - 10.1.2.2 Planar Over-the-Cell Routing . . . . . 377
    - 10.1.2.3 Over-the-Cell Routing Using Vacant Terminals 389
  - 10.1.3 Three-Layer Over-the-cell Routing . . . . . 396
  - 10.1.4 Multilayer OTC Routing . . . . . 398
  - 10.1.5 Performance Driven Over-the-cell Routing . . . . . 398
- 10.2 Via Minimization . . . . . 400
  - 10.2.1 Constrained Via Minimization Problem . . . . . 401
    - 10.2.1.1 Graph Representation of Two-Layer CVM Problem . . . . . 403
  - 10.2.2 Unconstrained Via Minimization . . . . . 407
    - 10.2.2.1 Optimal Algorithm for Crossing-Channel TVM Problem . . . . . 408
    - 10.2.2.2 Approximation Result for General  $k$ -TVM Problem . . . . . 409
    - 10.2.2.3 Routing Based on Topological Solution . . . . . 410
- 10.3 Summary . . . . . 410
- 10.4 Exercises . . . . . 411

**11 Clock and Power Routing 417**

- 11.1 Clock Routing . . . . . 418
  - 11.1.1 Clocking Schemes . . . . . 419
  - 11.1.2 Design Considerations for the Clocking System . . . . . 422
    - 11.1.2.1 Delay Calculation for Clock Trees . . . . . 423
  - 11.1.3 Problem Formulation . . . . . 426
    - 11.1.3.1 Design Style Specific Problems . . . . . 427
  - 11.1.4 Clock Routing Algorithms . . . . . 427
    - 11.1.4.1 H-tree Based Algorithm . . . . . 428
    - 11.1.4.2 The MMM Algorithm . . . . . 429
    - 11.1.4.3 Geometric Matching based Algorithm . . . . . 430
    - 11.1.4.4 Weighted Center Algorithm . . . . . 432
    - 11.1.4.5 Exact Zero Skew Algorithm . . . . . 433
    - 11.1.4.6 DME Algorithm . . . . . 436
  - 11.1.5 Skew and Delay Reduction by Pin Assignment . . . . . 439
  - 11.1.6 Multiple Clock Routing . . . . . 439
- 11.2 Power and Ground Routing . . . . . 440
- 11.3 Summary . . . . . 444
- 11.4 Exercises . . . . . 444

<b>12</b>	<b>Compaction</b>	<b>449</b>
12.1	Problem Formulation . . . . .	450
12.1.1	Design Style Specific Compaction Problem . . . . .	450
12.2	Classification of Compaction Algorithms . . . . .	451
12.3	One-Dimensional Compaction . . . . .	452
12.3.1	Constraint-Graph Based Compaction . . . . .	453
12.3.1.1	Constraint Graph Generation . . . . .	454
12.3.1.2	Critical Path Analysis . . . . .	460
12.3.1.3	Wire Jogging . . . . .	463
12.3.1.4	Wire Length Minimization . . . . .	463
12.3.2	Virtual Grid Based Compaction . . . . .	463
12.3.2.1	Basic Virtual Grid Algorithm . . . . .	464
12.3.2.2	Split Grid Compaction . . . . .	464
12.3.2.3	Most Recent Layer Algorithm . . . . .	467
12.4	$1\frac{1}{2}$ -Dimensional Compaction . . . . .	468
12.5	Two-Dimensional Compaction . . . . .	470
12.5.1	Simulated Annealing based Algorithm . . . . .	473
12.6	Hierarchical Compaction . . . . .	473
12.6.1	Constraint-Graph Based Hierarchical Compaction . . . . .	473
12.7	Recent trends in compaction . . . . .	474
12.7.1	Performance-driven compaction . . . . .	474
12.7.2	Compaction techniques for yield enhancement . . . . .	475
12.8	Summary . . . . .	476
12.9	Exercises . . . . .	476
<b>13</b>	<b>Physical Design Automation of FPGAs</b>	<b>479</b>
13.1	FPGA Technologies . . . . .	480
13.2	Physical Design Cycle for FPGAs . . . . .	485
13.3	Partitioning . . . . .	485
13.4	Routing . . . . .	489
13.4.1	Routing Algorithm for the Non-Segmented Model . . . . .	490
13.4.2	Routing Algorithms for the Segmented Model . . . . .	492
13.4.2.1	Basic Algorithm . . . . .	493
13.4.2.2	Routing Algorithm for Staggered Model . . . . .	494
13.5	Summary . . . . .	496
13.6	Exercises . . . . .	497
<b>14</b>	<b>Physical Design Automation of MCMs</b>	<b>501</b>
14.1	MCM Technologies . . . . .	502
14.2	MCM Physical Design Cycle . . . . .	505
14.3	Partitioning . . . . .	507
14.4	Placement . . . . .	510
14.4.1	Chip Array Based Approach . . . . .	512
14.4.2	Full Custom Approach . . . . .	512
14.5	Routing . . . . .	513
14.5.1	Classification of MCM Routing Algorithms . . . . .	514

14.5.2	Maze Routing . . . . .	514
14.5.3	Multiple Stage Routing . . . . .	515
14.5.3.1	Pin Redistribution Problem . . . . .	515
14.5.3.2	Layer Assignment . . . . .	517
14.5.3.3	Detailed Routing . . . . .	517
14.5.4	Topological Routing . . . . .	517
14.5.5	Integrated Pin Distribution and Routing . . . . .	519
14.5.6	Routing in Programmable Multichip Modules . . . . .	519
14.6	Summary . . . . .	521
14.7	Exercises . . . . .	521
	<b>Bibliography</b>	<b>525</b>
	<b>Author Index</b>	<b>563</b>
	<b>Subject Index</b>	<b>567</b>